

REMARKS

Claims 1-30 are pending. Claims 1-4, 8-11, 21 and 29 have been amended.

The Examiner objected to the title, abstract, and drawings for a number of reasons. Claims 8-14, 21-26 and 29-30 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1-3, 6, 15-17, 19 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Huang et al. (hereinafter "Huang"). Claims 1-30 were rejected under 35 U.S.C. § 102(e) as being anticipated by Taruishi et al. (hereinafter "Taruishi"). Claims 1-3 and 5-30 were rejected under 35 U.S.C. § 103(a) as being obvious over alleged Applicants' Admitted Prior Art (hereinafter called the "AAPA") in view of Huang. Claim 4 was rejected under 35 U.S.C. § 103(a) as being obvious over the AAPA in view of Huang and in further view of Yanagawa.

The title has been amended to overcome the objection to the title. Furthermore, the Abstract has been amended to overcome the objection to the Abstract. Regarding the objections to the drawings, the drawings have been changed to overcome the objections to the drawings. More specifically, Applicant submits with this Reply annotated and replacement sheets of drawings for the Examiner's approval. The Examiner contends that the sense amp control circuit 114 should be receiving the inverse of the delayed DQS signal. However, Applicant submits that the drawing is proper as currently labeled. Furthermore, Applicant submits that the read buffer latches 151 and 154 in Figure 11 do not necessarily receive the SCLK signal, and thus, this signal has not been shown in Figure 11. The specification has been amended, as suggested by the Examiner, to overcome the objections to the specification. Furthermore, the claims have been amended to overcome the objections to the claims. The §§ 112, 102 and 103 rejections are addressed below.

§ 112 Rejections:

The claims have been amended to address some of the § 112 rejections, such as the rejections directed to proper antecedent bases for "predetermined operation."

Objections were made to claims 8, 21 and 29 because, "it is not entirely clear how the amplifiers are enabled in response to a predetermined operation occurring." Office Action, 7. The Examiner suggests amending claims 8, 21 and 29 so that these claims recite that the amplifiers are enabled in response to the *beginning* of a predetermined operation occurring. (emphasis added). However, Applicant desires to maintain the breadth of these claims.

Claims do not need to describe *how* an action is performed to satisfy the second paragraph of section 112. Rather, section 112 sets forth two requirements: 1. the claims must set forth the subject matter that applicants regard as their invention; and 2. the claims must particularly point out and distinctly define the metes and bounds of the subject matter that will be protected by the patent grant. M.P.E.P. § 2171. The Office Action fails to set forth why claims 8, 21 and 29 fail either of these requirements; and thus, Applicant submits that claims 8, 21 and 29, as amended, satisfy the second paragraph of section 112. It is noted that claim breadth is not be equated with indefiniteness. M.P.E.P. § 2173.04.

§§ 102 and 103 Rejections of Claims 1-7:

Independent claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Huang. Huang fails to teach or even suggest selectively disabling the amplification of data signals that are received *from* a memory bus, as set forth in amended claim 1.

To the contrary, Huang teaches a power consumption technique/circuit for use with data signals that are being furnished *to* a memory bus. In Huang, a sense/output circuit switches off some power-consuming components immediately after a requested data output is completed. See Huang, Abstract. The sense/output circuit includes a sense amplifier, having two stages. The first stage is coupled to a pair of output bit lines of the memory device and amplifies the differential data signal representative of a bit of data on those lines. However, the output bit

lines are in the memory itself and are not a part of the memory bus. The second stage of the sense amplifier merely amplifies the output of the first stage and provides its output signals to a pair of data lines of the memory bus. Thus, the data signal amplified by the sense amplifier is not received from the memory bus. Instead, it is received from the memory itself, and the output of the sense amplifier is provided to the memory bus.

Therefore, reconsideration and withdrawal of the 102(b) rejection of independent claim 1, as amended, in view of Huang is respectfully requested.

Independent claim 1 was also rejected under 35 U.S.C. § 102(e) as being anticipated by Taruishi. Taruishi fails to teach or suggest selectively disabling the amplification of data signals received *from the memory bus* in response to the absence of a predetermined operation occurring over the memory bus, as set forth in amended claim 1.

In Taruishi, only one memory bank whose operation is selected is capable of memory operation. The sense amplifiers and the write amplifiers are not activated for the non-selected memory banks. See Taruishi, col. 6, lines 36-40. A sense amplifier is defined in Taruishi to be “an amplifier circuit for detecting and amplifying a small potential difference developed between the complementary bit lines....” See Taruishi, col. 5, lines 61-64. A write amplifier is defined in Taruishi to be “a circuit for amplifying the differences in potential between the adjacent complementary bit lines....” See Taruishi, col. 6, lines 4-8. However, the complementary bit lines are in the memory itself and are not a part of the memory bus. Thus, the data signals amplified by the sense amplifiers and the write amplifiers are not received *from* the memory bus.

Therefore, reconsideration and withdrawal of the 102(e) rejection of independent claim 1, as amended, in view of Taruishi is respectfully requested.

Independent claim 1 was rejected under 35 U.S.C. § 103(a) as being obvious over the alleged AAPA in view of Huang.

To establish obviousness based on a combination of references, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1316 (Fed. Cir. 2000); M.P.E.P. § 2143. For a *prima facie* case of obviousness, the Examiner must support the allegation of a

suggestion or motivation in the art for the combination of references with a specific cite to some portion of a cited reference, as “obviousness cannot be predicated on what is unknown.” *In re Spormann*, 150 U.S.P.Q. 449, 452 (C.C.P.A. 1966); *See Ex parte Gambogi*, 62 U.S.P.Q.2d 1209, 1212 (Bd. Pat. App. & Int. 2001) and *In re Rijckaert*, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993).

The Office Action fails to show where the prior art contains the alleged suggestion or motivation to combine the AAPA and Huang. Therefore, reconsideration and withdrawal of the 103(a) rejection of independent claim 1, as amended, is respectfully requested.

Claims 2-7 are patentable for at least the reason that these claims depend from an allowable claim.

§§ 102 and 103 Rejections of Claims 8-14:

Independent claim 8 was rejected under 35 U.S.C. § 102(e) as being anticipated by Taruishi. However, Taruishi fails to teach or suggest selectively enabling the amplification of data signals received *from the memory bus* in response to a predetermined operation occurring over the memory bus, as set forth in amended claim 8.

In Taruishi, the sense amplifiers and the write amplifiers amplify potential differences developed between complementary bit lines. See col. 5, lines 61-64 and col. 6, lines 4-8. However, the complementary bit lines are in the memory itself and are not a part of the memory bus. Thus, the data signals amplified by the sense amplifiers and the write amplifiers are not received from the memory bus.

Therefore, reconsideration and withdrawal of the 102(e) rejection of independent claim 8, as amended, in view of Taruishi is respectfully requested.

Independent claim 8 was also rejected under 35 U.S.C. § 103(a) as being obvious over the alleged AAPA in view of Huang. However, the Office Action fails to show where the prior art contains the alleged suggestion or motivation to combine the AAPA and Huang.

Therefore, reconsideration and withdrawal of the 103(a) rejection of independent claim 8, as amended, is respectfully requested.

Claims 9-14 are patentable for at least the reason that these claims depend from an allowable claim.

§§ 102 and 103 Rejections of Claims 15-20:

Independent claim 15 was rejected under 35 U.S.C. § 102(b) as being anticipated by Huang. However, Huang fails to teach or suggest amplifiers to amplify data signals received *from a memory bus*, as set forth in claim 15.

In Huang, the data signals amplified by the amplifiers are not received from a memory bus. Instead, the data signals are received from output bit lines in the memory itself.

Therefore, reconsideration and withdrawal of the 102(b) rejection of independent claim 15 in view of Huang is respectfully requested.

Independent claim 15 was also rejected under 35 U.S.C. § 102(e) as being anticipated by Taruishi. However, Taruishi fails to teach or suggest a second circuit to selectively disable the amplification of data signals received *from the memory bus* in response to the absence of a predetermined operation occurring over the memory bus, as set forth in claim 15.

In Taruishi, the sense amplifiers and the write amplifiers are not activated for the non-selected memory banks. See Taruishi, col. 6, lines 37-40. The sense amplifiers and the write amplifiers amplify potential differences developed between complementary bit lines. See Taruishi, col. 5, lines 61-64 and col. 6, lines 4-8. However, the complementary bit lines are in the memory itself and are not a part of the memory bus. Thus, the data signals amplified by the sense amplifiers and the write amplifiers are not received *from* the memory bus.

Therefore, reconsideration and withdrawal of the 102(e) rejection of independent claim 15 in view of Taruishi is respectfully requested.

Independent claim 15 was rejected under 35 U.S.C. § 103(a) as being obvious over the Applicants' admitted prior art in view of Huang. However, the Office Action fails to show where the prior art contains the alleged suggestion or motivation to combine the AAPA and Huang.

Therefore, reconsideration and withdrawal of the 103(a) rejection of independent claim 15 is respectfully requested.

Claims 16-20 are patentable for at least the reason that these claims depend from an allowable claim.

§§ 102 and 103 Rejections of Claims 21-26:

Independent claim 21 was rejected under 35 U.S.C. § 102(e) as being anticipated by Taruishi. However, Taruishi fails to teach or suggest a second circuit to selectively enable the amplification of data signals received *from the memory bus* in response to a predetermined operation occurring over the memory bus, as set forth in amended claim 21.

In Taruishi, the sense amplifiers and the write amplifiers amplify potential differences developed between complementary bit lines. See col. 5, lines 61-64 and col. 6, lines 4-8. However, the complementary bit lines are in the memory itself and are not a part of the memory bus. Thus, the data signals amplified by the sense amplifiers and the write amplifiers are not received *from the memory bus*.

Therefore, reconsideration and withdrawal of the 102(e) rejection of independent claim 21, as amended, in view of Taruishi is respectfully requested.

Independent claim 21 was also rejected under 35 U.S.C. § 103(a) as being obvious over the alleged AAPA in view of Huang. However, the Office Action fails to show where the prior art contains the alleged suggestion or motivation to combine the AAPA and Huang.

Therefore, reconsideration and withdrawal of the 103(a) rejection of independent claim 21, as amended, is respectfully requested.

Claims 22-26 are patentable for at least the reason that these claims depend from an allowable claim.

§§ 102 and 103 Rejections of Claims 27-28:

Independent claim 27 was rejected under 35 U.S.C. § 102(e) as being anticipated by Taruishi. Independent claim 27 also distinguishes over Taruishi for reasons similar to those set forth above with respect to independent claim 15, as amended.

Therefore, reconsideration and withdrawal of the 102(e) rejection of independent claim 27 is respectfully requested.

Independent claim 27 was rejected under 35 U.S.C. § 103(a) as being obvious over the alleged AAPA in view of Huang. However, the Office Action fails to show where the prior art contains the alleged suggestion or motivation to combine the AAPA and Huang.

Therefore, reconsideration and withdrawal of the 103(a) rejection of independent claim 27 is respectfully requested.

Claim 28 is patentable for at least the reason that it depends from an allowable claim.

Rejection of Claims 29-30:

Independent claim 29 was rejected under 35 U.S.C. § 102(e) as being anticipated by Taruishi. Independent claim 29, as amended, also distinguishes over Taruishi for reasons similar to those set forth above with respect to independent claim 21, as amended.

Therefore, reconsideration and withdrawal of the 102(e) rejection of independent claim 29, as amended, is respectfully requested.

Independent claim 29 was rejected under 35 U.S.C. § 103(a) as being obvious over the alleged AAPA in view of Huang. Independent claim 29, as amended, also distinguishes over the Applicants' admitted prior art and Huang for reasons similar to those set forth above with respect to independent claim 1, as amended.

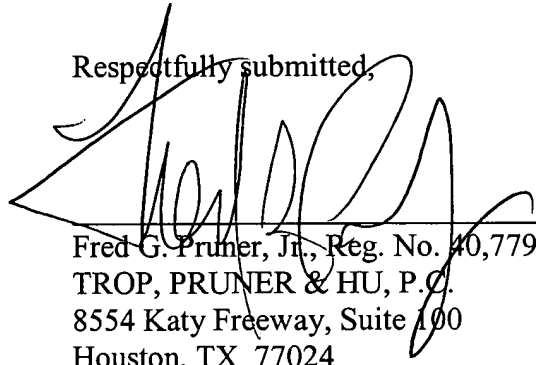
Therefore, reconsideration and withdrawal of the 103(a) rejection of independent claim 29, as amended, is respectfully requested.

Claim 30 is patentable for at least the reason that it depends from an allowable claim.

CONCLUSION

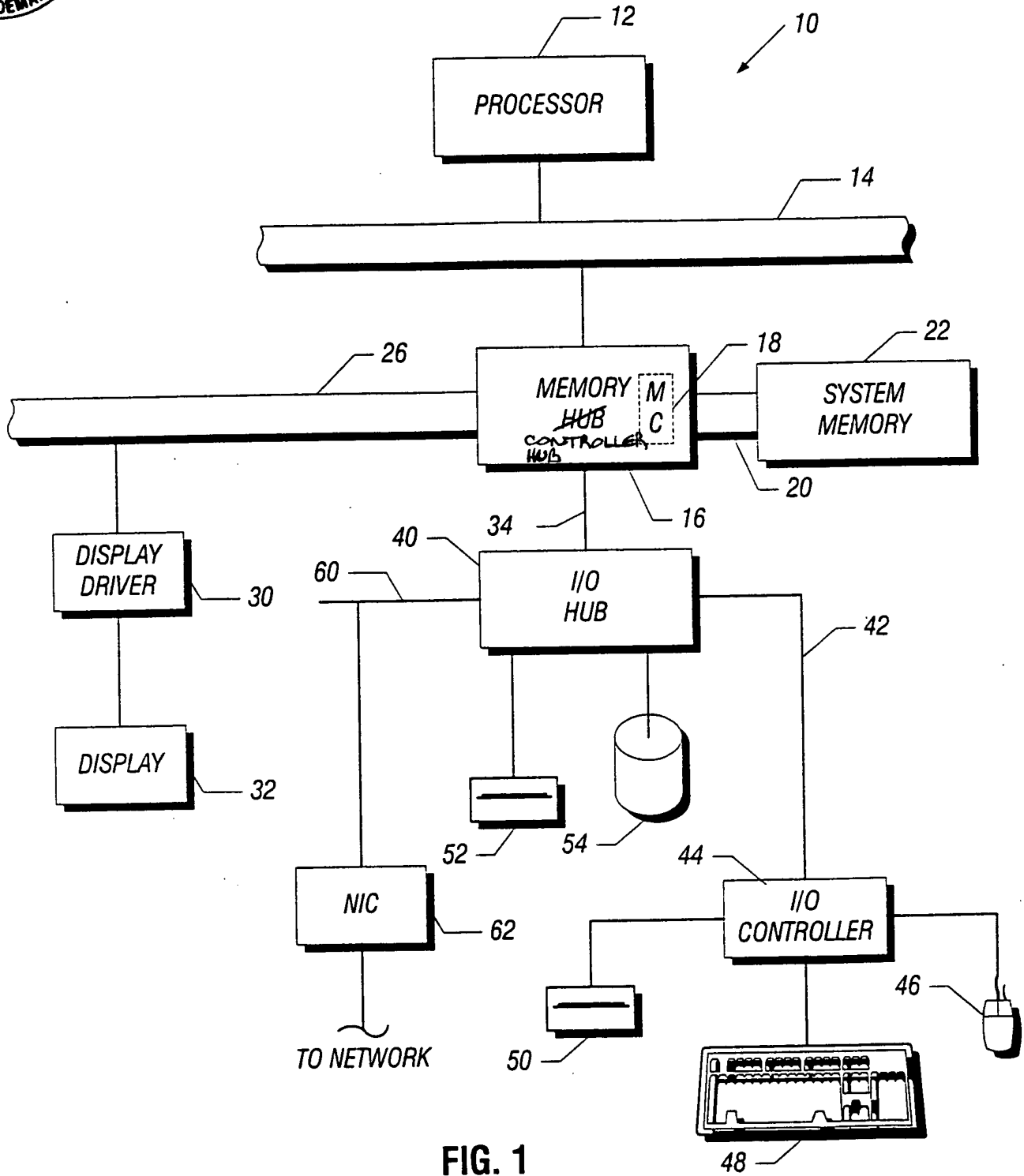
In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0668US).

Respectfully submitted,



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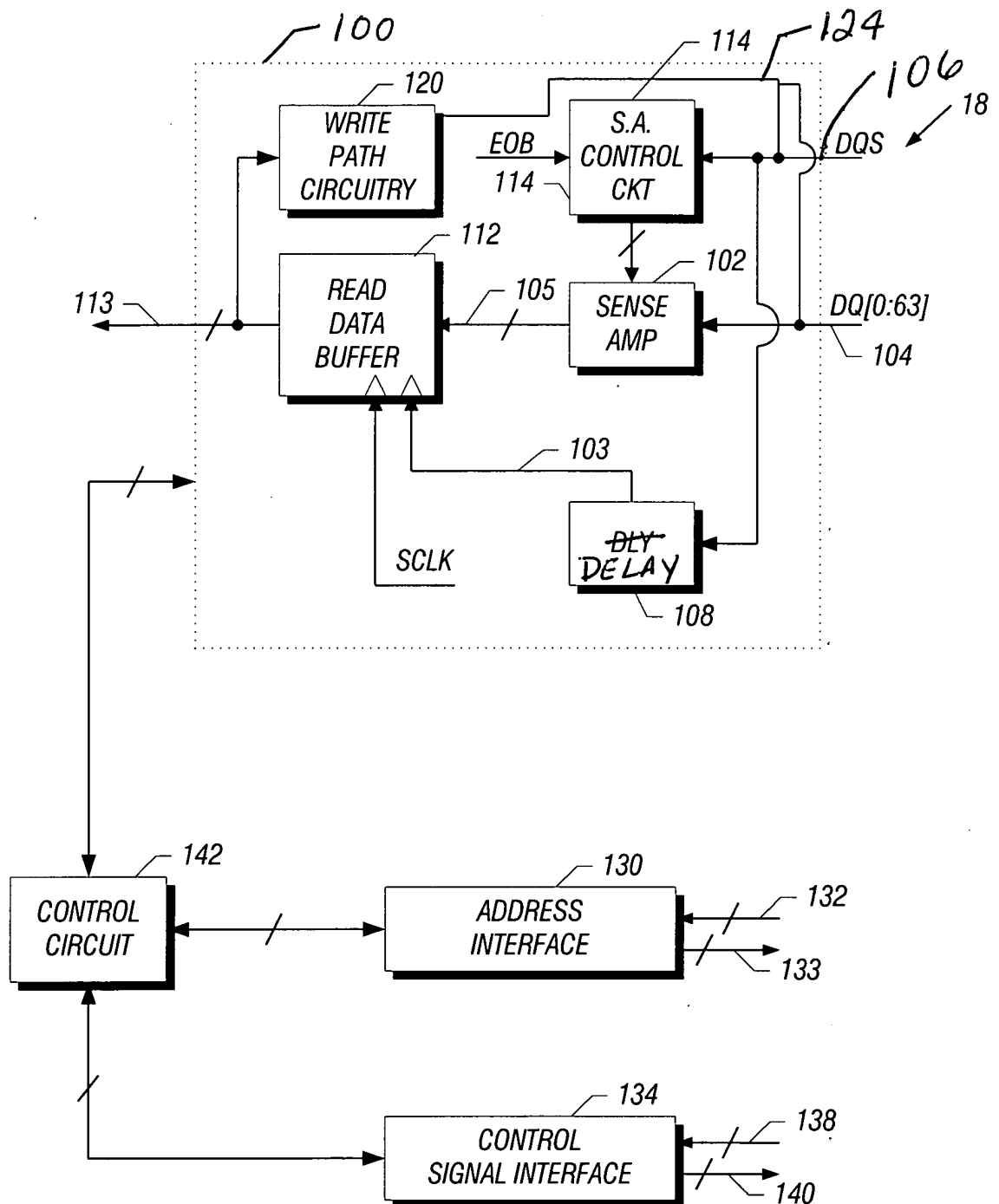
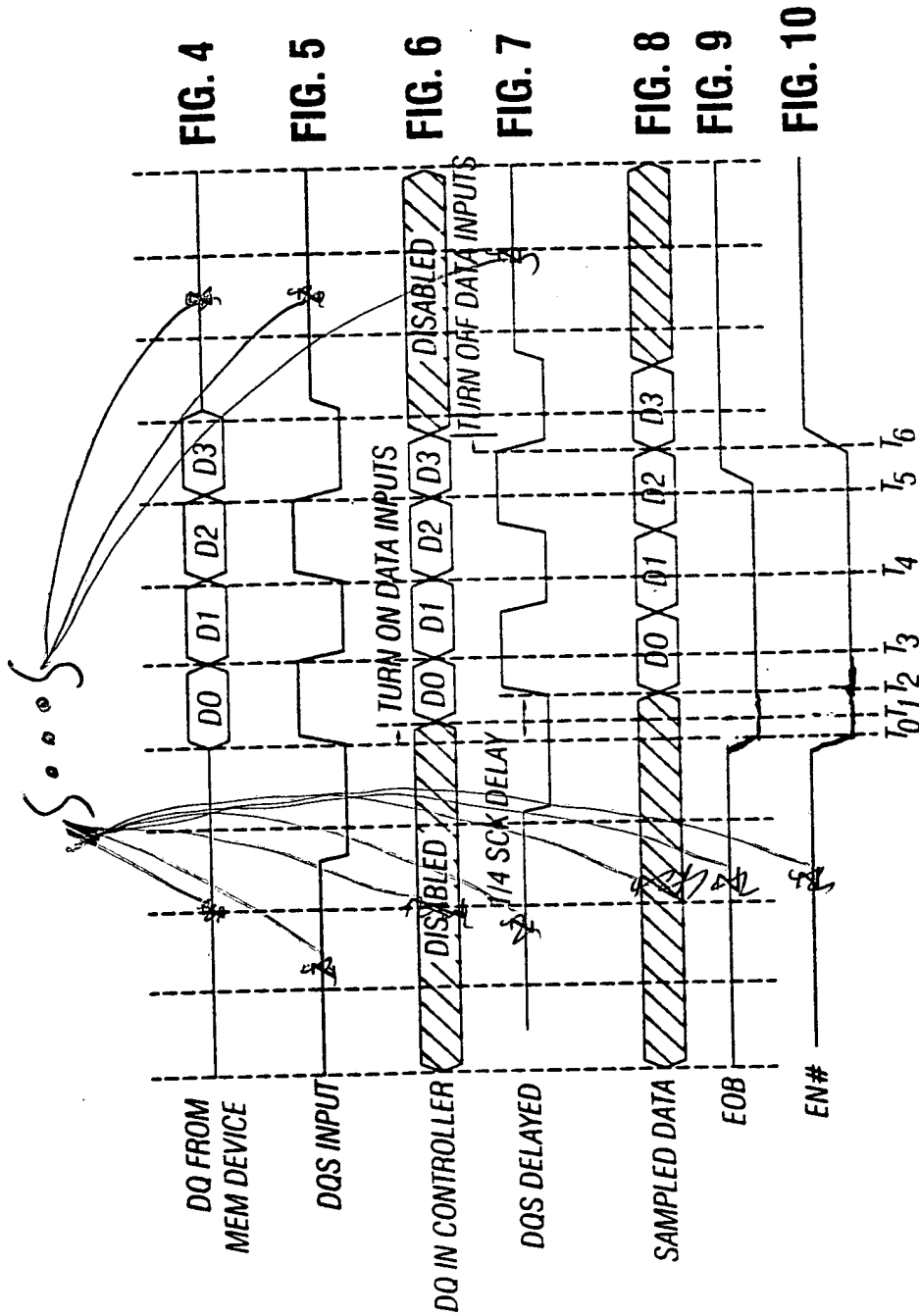


FIG. 3



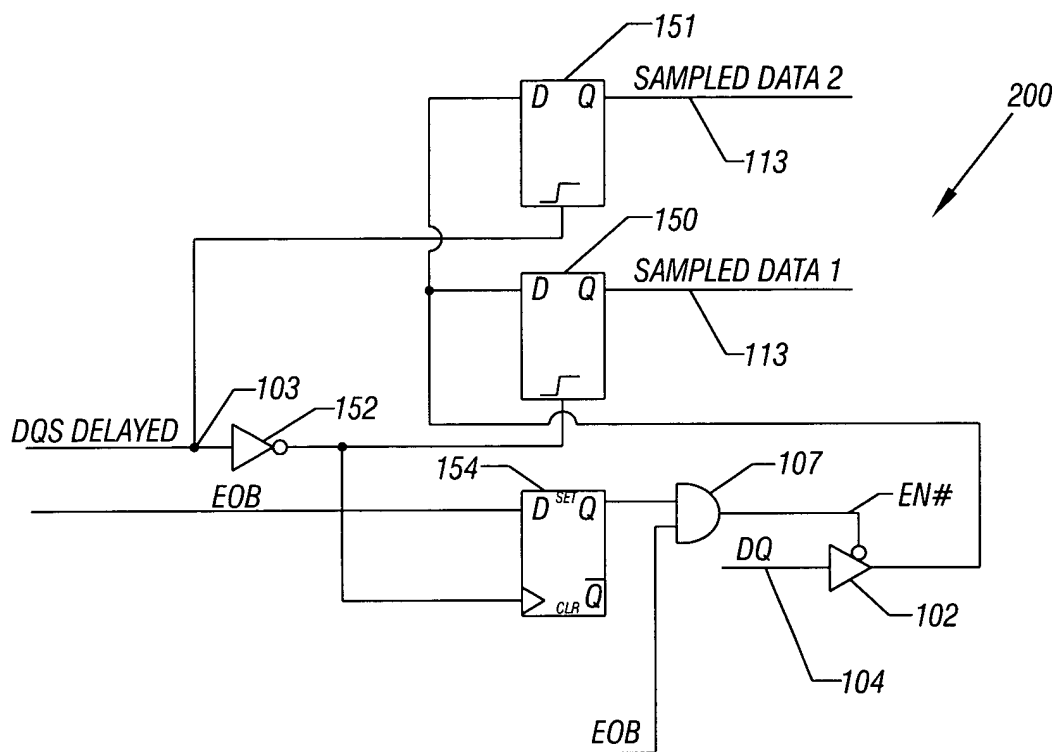


FIG. 11

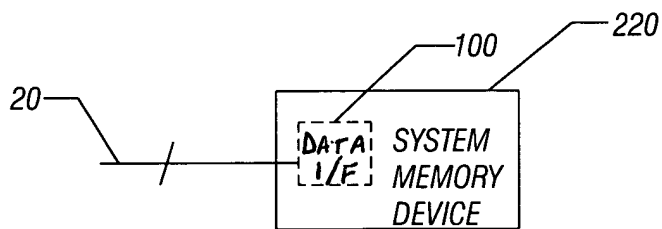


FIG. 12